CLAIMS:

1. A flyback converter, comprising a primary side input circuit (1), having a primary winding (2) wound on a transformer (3) and a primary switch element (4) in series with the primary winding (2), a first output circuit (5), having a first secondary winding (6), wound on the transformer (3) and connected in series with a rectifying element (7) and a secondary switch element (8), and at least a second output circuit (10), having a second secondary winding (11), wound on the transformer (3) and connected in series with a rectifying element (12), wherein said first output circuit (5) comprises means (24; 25; 27; 31) for increasing the inductance in the first output circuit (5).

2. A flyback converter according to claim 1, wherein said means for increasing the inductance in the first secondary output circuit comprises means (25; 27; 31) for increasing the leakage inductance of the first secondary winding (6).

3. A flyback converter according to claim 2, wherein the first secondary winding (6) is primarily wound around a first leg (26) of the transformer (3) and wherein said means for increasing the leakage inductance of the first secondary winding (6) comprises at least one turn (27) in the first secondary winding (6) enclosing a second leg (28) of the transformer (3).

4. A flyback converter according to claim 2, wherein said means for increasing the leakage inductance of the first secondary winding (6) comprises a gap (25) between the primary winding (2) and the first secondary winding (6).

5. A flyback converter according to claim 1, wherein said means for increasing the inductance in the first secondary output circuit (5) comprises an auxiliary inductance (24), connected in series with the first secondary winding, and a freewheeling diode (29), for allowing a current to continue to flow through the auxiliary inductance when the secondary switch (8) is opened.

6. A flyback converter according to any of the preceding claims, further comprising control means (30) for variably controlling the output of the first secondary output circuit (5).